CX32L003 UserManual 1.0.2 FlashDetails EN

04 Sep 2023

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10 Flash controller (Flash)

10.1 Flash Controller Overview

This chip contains a 64K / 32K Byte capacity embedded Flash memory, including a 128 / 64 sector MainArray area.
An 8 sector NVR area. The capacity of each sector is 512 Byte. The MainArray area of Flash is for users to use.
Can store user-developed programs and data. In the NVR area, one sector is used to store system configuration and one sector is used to store options.
bytes, and the remaining 6 sectors are used to store the system's ISP program. This module supports erasing, programming and reading of Flash memory
operate. In addition, this module supports the protection of flash memory erasure and write protection of control registers.

10.2 Flash structure block diagram

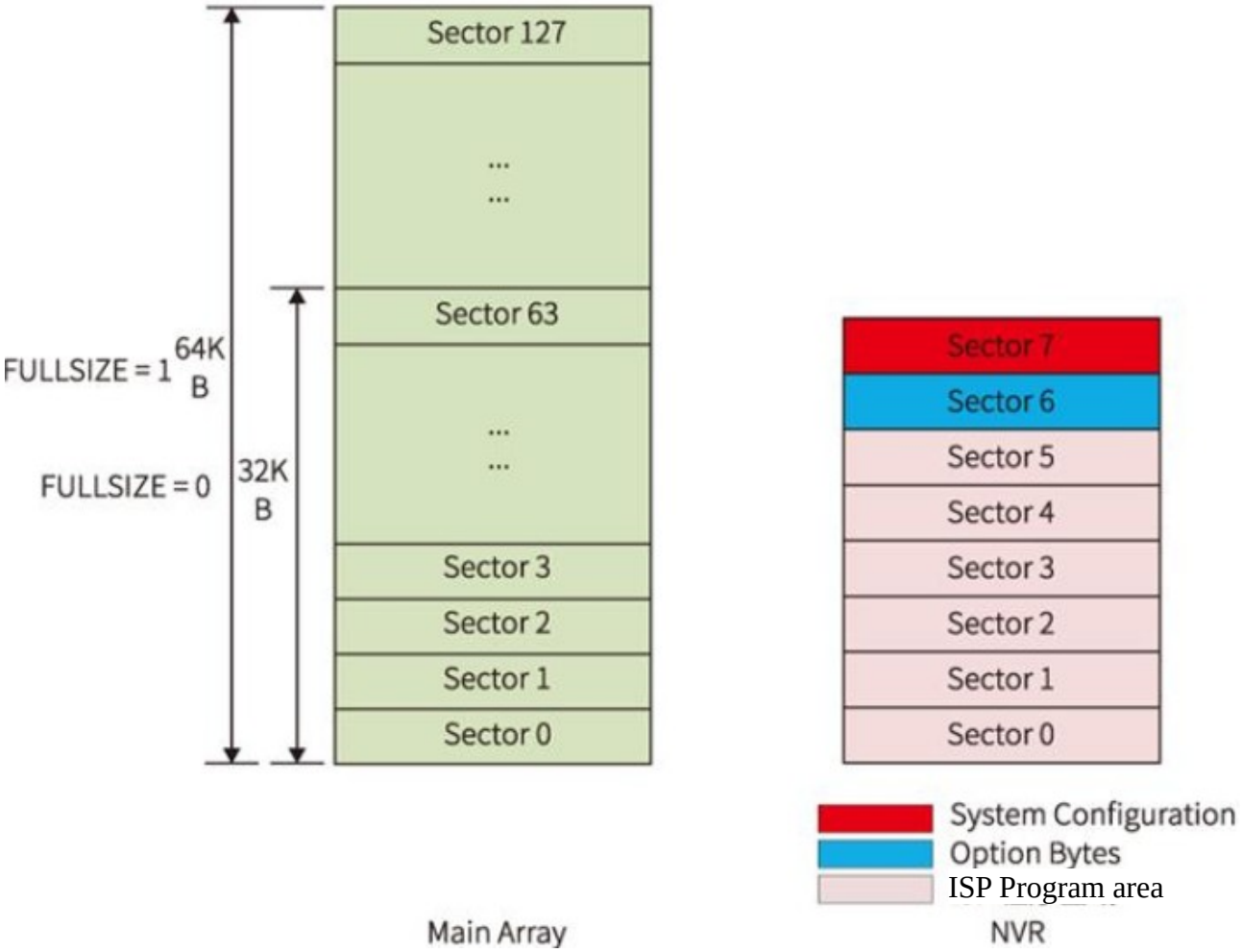

Figure 10-1 Flash structure block diagram

The Main Array area is used to store user code.

Sector 0~5 of the NVR area are used to store the system ISP (in-system programmable) code provided by the manufacturer. The user can

For applications developed by downloading the ISP code, the user program cannot read or erase the ISP code. NVR area

Sector 6 is the option byte area, which is used by users to configure some system functions. Sector 7 of the NVR area is the system configuration area. Used to store system configuration values.

10.3 Function description

This controller supports three bit width read and write operations of Flash: byte (8bits), half-word (16bits), and word (32bits).
Notice:
The address of byte operation must be aligned by byte, and the target address of half-word operation must be aligned by half-word (the lowest bit of the address is 0), the target address of word operation must be word aligned (the lowest two bits of the address are 0).
If the address of the read or write operation does not follow the bit width specifies alignment, the operation is invalid, and the system will enter a hard fault error interrupt.

10.3.1 Erase operation

10.3.1.1 Sector Erase

The Sector erasure operation steps are shown in the figure below:
Algorithm

Step1: Set FLASH_CR.OP[1:0]=2'b10 (value decimal 2)
Step2: Write operation to target address
Step3: FLASH_CR.BUSY="0"? => Yes wait until it is equal to 0
Step4: Next operation

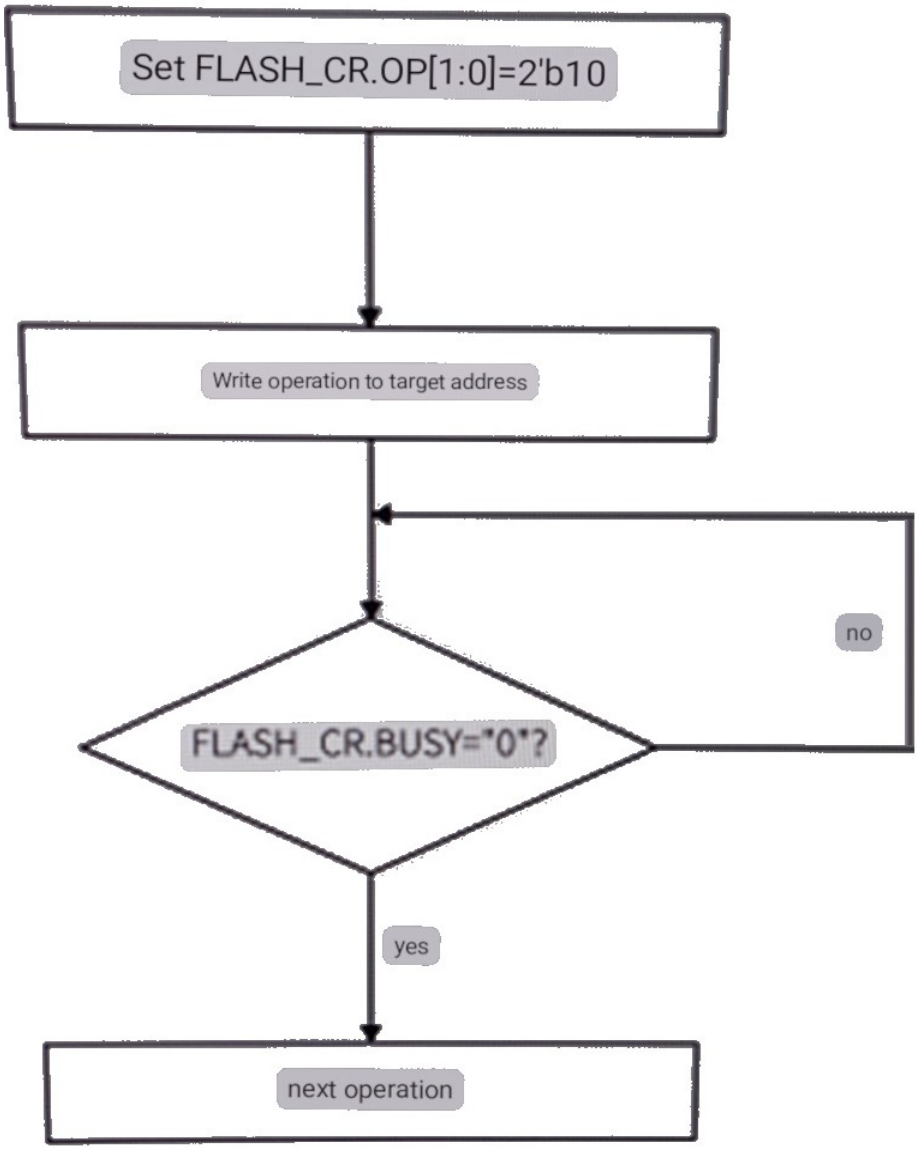

Figure 10-2 Sector erase operation steps

10.3.1.2 Chip Erase

Chip erase operation steps are shown in the figure below:

Step1: Set FLASH_CR.OP[1:0]=2'b11 (value decimal 3)
Step2: Write operation to target address
Step3: FLASH_CR.BUSY="0"? => Yes wait until it is equal to 0
Step4: Next operation

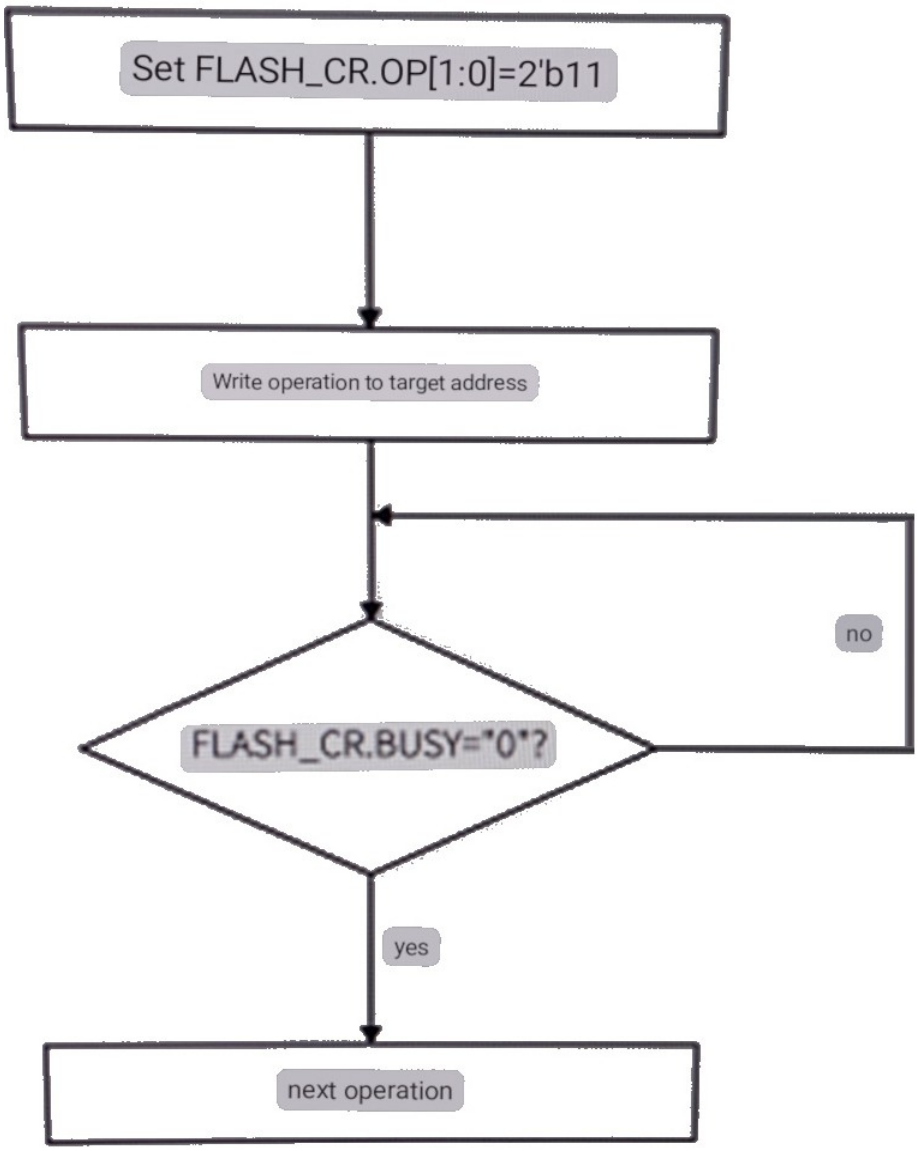

Figure 10-3 chip erase operation steps

10.3.2 Write operations

The writing operation steps are shown in the figure below:

Step1: Set FLASH_CR.OP[1:0]=2'b01 (value decimal 1)
Step2: Write operation to target address
Step3: FLASH_CR.BUSY="0"? => Yes wait until it is equal to 0
Step4: Next operation

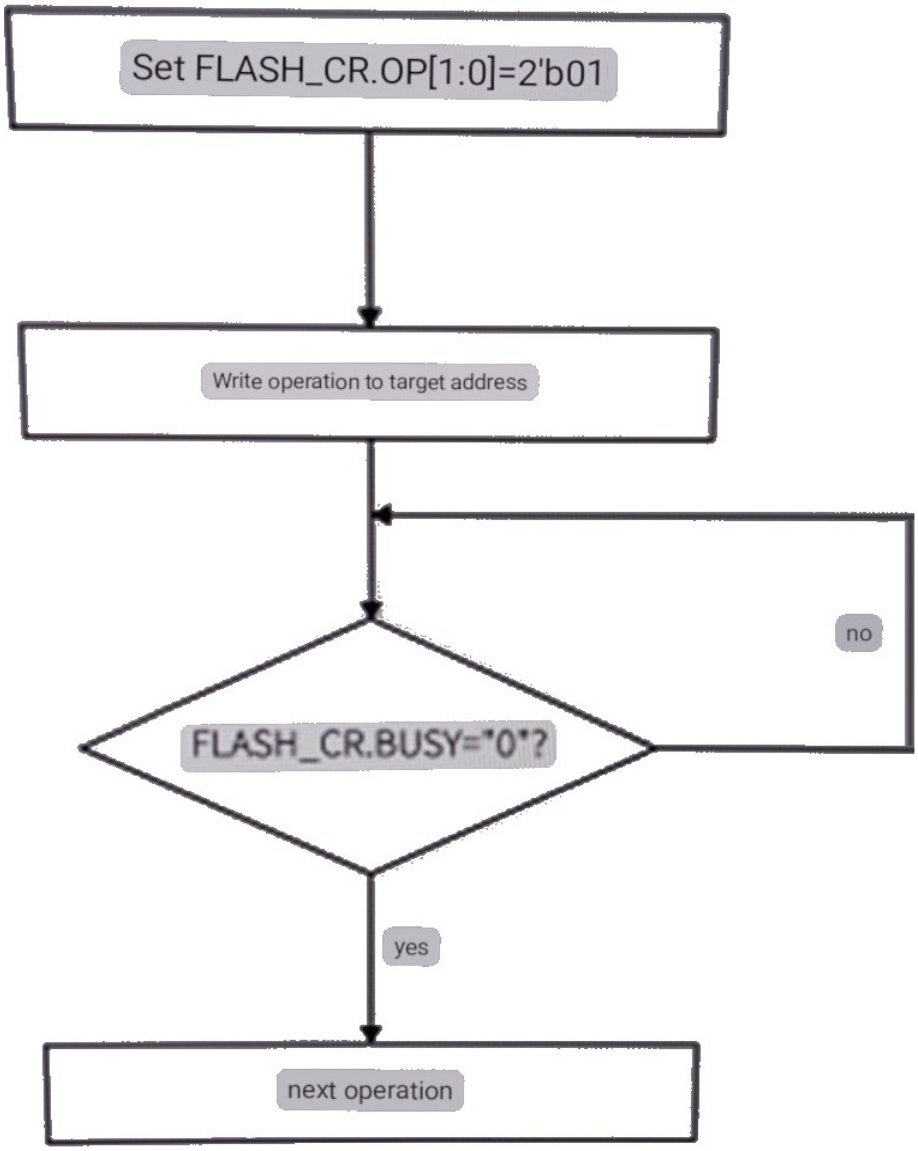

Figure 10-4 Writing operation steps

Notice:
1. If the current write operation instruction is executed in Flash, the CPU will suspend the action of fetching and executing instructions, and automatically waits for the Flash to
After the BUSY state ends, continue fetching and executing instructions.
2. If the current write operation instruction is executed in RAM, the CPU will not stop fetching and executing any operations on Flash.
Previously, the software had to determine whether the BUSY state of Flash ended.

10.3.3 Read operation

The operation of reading Flash is the same as that of CPU reading SRAM memory, and there are no special requirements. The maximum read speed of the on-chip Flash of this chip
is 35ns, and the accuracy after on-chip HIRC trimming is ±1% (typ.), which translates into the fastest CPU single-cycle reading time of 41.3ns, so this chip meets the single-cycle read operation of Flash when the CPU uses the on-chip HIRC as the clock source.

10.3.4 Erase and write time

Flash memory has strict time requirements for the control signals of erasure and programming operations, and the effective time of the control signals exceeds the design requirements.
Will cause erasure and programming operations to fail. This chip sets the Flash sector erase time register (Flash_TSERASE), Flash the three registers of chip erase time register (Flash_TMERASE) and Flash programming time register (Flash_TPROG) can be divided in half.
Adjust sector, chip erase and program (write) times.
Note: During the CP stage, the chip will test the erase and programming time parameters of the Flash and write them into the system parameter configuration area.
After power-on, the circuit will automatically load these parameters into the sector, chip erase time register and programming time register, so generally
In this case, it is not recommended to change these set erase and write time parameters.

10.3.5 Erase and write protection

10.3.5.1 Erase and write protection bit

The entire 64K Byte Flash memory is divided into 128 sectors.
In order to prevent accidental erasing and writing operations in the application from changing the content, a total of 64 erase and write protection bits are set, and each erase and write protection bit is responsible for protecting 2 sector areas with protection bit register.
The default value of Flash_SLOCK.SLOCK0/1[31:0] is "0000_0000", which means erasing is not allowed, when we modify the corresponding protection bit to "1", the sector can be erased.
When any sector in the Flash memory is protected from erasure and write, the chip of the Flash memory Erase and write will also be automatically protected by the controller, and alarm flags and interrupt signals will occur.
If you need to erase the chip, you must modify the protection, the value of the guard bit register Flash_SLOCK.SLOCK0/1[31:0] is "0xFFFFFFFF".

10.3.5.2 PC address erasure protection

When the CPU runs a program in Flash, it will encounter a situation: the currently running PC pointer just falls on the sector where the software is erasing the Flash.
Within the address range, the erase and write operation will also be automatically blocked by the controller, and an alarm flag and interrupt signal will be generated.

10.3.5.3 Register write protection

In order to prevent accidental Flash erasing and writing operations from changing the content of Flash when application is running, the writing and erasing operations of the Flash controller register are protected by FLASH_BYPASS register.
During operation the write/erase operation to Flash must be modified using the FLASH_BYPASS write sequence method.
The specific operation steps are shown in the figure below:

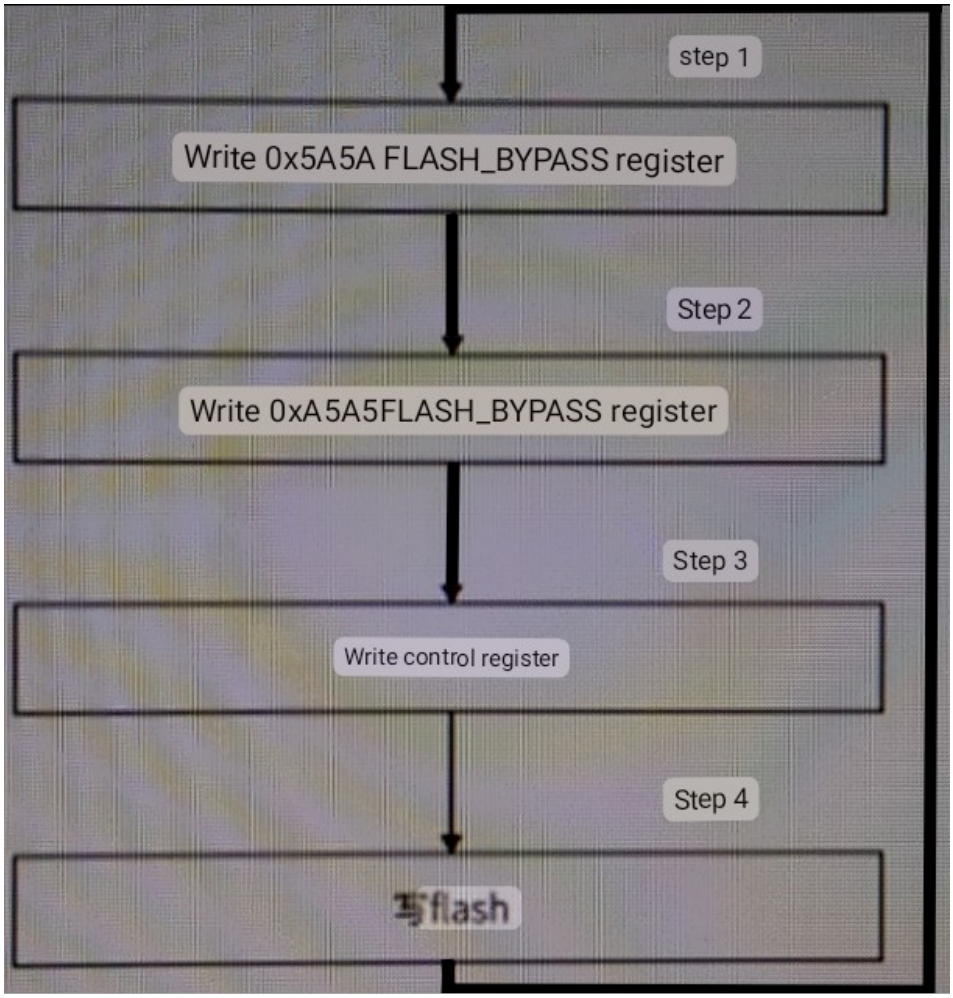

Figure 10-5 Write register BYPASS sequence

Notice:
No other write operations can be inserted between steps 1~4, otherwise the BYPASS sequence operation will be invalid and 0x5A5A & 0xA5A5 FLASH_BYPASS registers needs to be written again.

11 Revision

Date	Version	Description	Author
04 Sep 2023	V0.1	First version	Benjamin Vernoux